Indira Gandhi Delhi Technical University For Women
Department of Electronics and Communication Engineering
(Formerly Indira Gandhi Institute of Technology)
(Established by Govt. of Delhi vide Act 09 of 2012)

May 21, 2018

Walk-in-Interview for the post of Guest Lecturer and Research Associate under SMDP-C2SD (On Contract Basis)

Applications are invited from research oriented candidates for the position of Guest Lecturer under the project titled **"Special Manpower Development Program for Chip-to-System Design (C2SD)"** sponsored by Department of Electronics and Information Technology, Ministry of Communications & Information Technology, Government of India. Detail of the said post is as follows:

S. No.	Post	Essential Qualification	Emoluments
1	Guest Lecturer (One Post)	B.E./B.Tech./M.Sc./M.Tech. in Electronics & Communication/ Electrical & Electronics/ VLSI Design with first class, or its equivalent grade from a reputed Institute. A sound knowledge of VLSI and relevant software Cadence/Synopsys/Mentor Graphics is must. **Desirable Qualification:** Ph.D. or Gate/NET Qualified	Rs. 40,000 per month
2	Research Associate (One Post)	B.E./B.Tech. in Electronics & Communication/ Electrical & Electronics with first class, or its equivalent grade from a reputed Institute. A sound knowledge of Image Processing and Python is must.	Rs. 20,000 per month

General Terms and Conditions:

1) Both male and female candidates can apply for the above-mentioned posts.
2) The candidate should bring and submit the duly signed application form at the time of interview.
3) A photocopy of all the supporting documents should be attached with the application form and originals may be produced for verification purpose.
4) The position is purely on temporary basis for a period of 06 months. The duration can be extended depending upon the satisfactory performance and provision under the project.
5) Selection committee reserves the right to fix suitable criteria for selection of candidates.
6) No TA/DA will be provided to candidates for appearing in the Interview.
7) The candidates are requested to regularly check the university website for further proceedings, if any.
8) Date & Time for Interview: 5th June 2018 at 12.00 a.m.
   E-106, VLSI Lab,
   Electrical Engineering Block
   IGDTUW

Chief Investigator
SMDP-C2SD Project